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1 PASM: a reconfigurable parallel system for image processing
Howard Jay Siegel, Thomas Schwederski, Nathaniel J. Davis, James T. Kuehn
September 1984 **ACM SIGARCH Computer Architecture News**, Volume 12 Issue 4
Full text available: pdf(1.67 MB) Additional Information: full citation, abstract, references

PASM is a multifunction partitionable SIMD/MIMD system being designed at Purdue for parallel image understanding. It is to be a large-scale, dynamically reconfigurable multimicroprocessor system, which will incorporate over 1,000 complex processing elements. Parallel algorithm studies and simulations have been used to analyze application tasks in order to guide design decisions. A prototype of PASM is under construction (funded by an equipment grant from IBM), including 30 Motorola MC68010 proce ...

2 Synthetic aperture radar image processing on parallel supercomputers
Steve Plimpton, Gary Mastin, Denni Ghiglia
August 1991 **Proceedings of the 1991 ACM/IEEE conference on Supercomputing**
Full text available: pdf(995.65 KB) Additional Information: full citation, references, index terms

3 Dynamic load balancing of data parallel applications on a distributed network
Mounir Hamdi, Chi-Kin Lee
July 1995 **Proceedings of the 9th international conference on Supercomputing**
Full text available: pdf(1.06 MB) Additional Information: full citation, references, index terms

4 Session 12: languages and runtime libraries: Communication and memory requirements as the basis for mapping task and data parallel programs
Jaspal Subhlok, David R. O'Hallaron, Thomas Gross, Peter A. Dinda, Jon Webb
November 1994 **Proceedings of the 1994 ACM/IEEE conference on Supercomputing**
Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references

For a wide variety of applications, both task and data parallelism must be exploited to achieve the best possible performance on a multicomputer. Recent research has underlined the importance of exploiting task and data parallelism in a single compiler framework, and such a compiler can map a single source program in many different ways onto a parallel machine. The tradeoffs between task and data parallelism are complex and depend on the characteristics of the program to be executed, most signif ...

5 Realization of a programmable parallel DSP for high performance image processing applications
Jens Peter Wittenburg, Willm Hinrichs, Johannes Kneip, Martin Ohmacht, Mladen Bereković,

Hanno Lieske, Helge Kloos, Peter Pirsch
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(2.35 MB) Publisher Site   Additional Information: full citation, abstract, references, citings, index terms

Architecture and design of the HiPAR-DSP, a SIMD controlled signalprocessor with parallel data paths, VLIW and novel memory design.The processor architecture is derived from an analysis of thetarget algorithms and specified in VHDL on register transfer level.A team of more than 20 graduate students covered the whole designprocess, including the synthesizable VHDL description, synthesis,routing and backannotation as the development of a complete softwaredevelopment environment.The 175mm{2}, 0.5¿m ...

6 Latency and bandwidth considerations in parallel robotics image processing
J. A. Webb
December 1993 **Proceedings of the 1993 ACM/IEEE conference on Supercomputing**

Full text available: pdf(892.99 KB)   Additional Information: full citation, references, citings, index terms

7 A parallel pipelined data flow coprocessor
J. T. Canning, R. Miner
February 1989 **Proceedings of the 17th conference on ACM Annual Computer Science Conference**

Full text available: pdf(594.17 KB)   Additional Information: full citation, abstract, references, citings, index terms

A parallel pipelined data flow coprocessor has been developed for the 68000 based Commodore Amiga workstation. The coprocessor, based on Nippon Electric Corporation's &mgr;PD7281 Image Pipelined Processor (ImPP), was designed as an algorithm processor for numerically intensive applications such as image processing, image synthesis, and numerical analysis. The coprocessor can accomodate up to seven of the 5-MIPS ImPP's providing over 30 MIPS of processing power to dedicated ...

8 Session 10: engineering applications II: Adaptive data parallel methods for ecosystem monitoring
Charles J. Turner, Jennifer G. Turner
November 1994 **Proceedings of the 1994 ACM/IEEE conference on Supercomputing**

Full text available: pdf(976.61 KB)   Additional Information: full citation, abstract, references

Biological diversity is decreasing at an alarming rate worldwide. Improved ecosystem monitoring can help detect problems in time to intervene. Earth orbiting satellites, collecting terabytes of imagery daily, can support effective monitoring of many habitats. Data parallelism is ideal for many automated image analysis algorithms, but less natural for the complex spatial structure of most ecosystems. This paper presents a coarse-to-fine processing framework based on a set of spatial transformatio ...

9 A new model for integrated nested task and data parallel programming
Jaspal Subhlok, Bwolen Yang
June 1997 **ACM SIGPLAN Notices , Proceedings of the sixth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 32 Issue 7

Full text available: pdf(1.27 MB)   Additional Information: full citation, abstract, references, citings, index terms

High Performance Fortran (HPF) has emerged as a standard language fordata parallel computing. However, a wide variety of scientific applications are best programmed by a combination of task and data parallelism. Therefore, a good model of task parallelism is important for continued success of HPF for parallel programming. This paper presents a task parallelism model that is simple, elegant, and relatively easy to implement in an HPF environment. Task parallelism is exploited by mechanisms for di ...

10 A Hybrid Architectural Style for Distributed Parallel Processing of Generic Data Streams
Alexandre R. J. Francois
May 2004 **Proceedings of the 26th International Conference on Software Engineering**
Full text available: pdf(250.47 KB) Additional Information: full citation, abstract

Immersive, interactive applications grouped under theconcept of Immersipresence require on-line processing andmixing of multimedia data streams and structures. One criticalissue seldom addressed is the integration of differentsolutions to technical challenges, developed independentlyin separate fields, into working systems, that operateunder hard performance constraints. In order to realizethe Immersipresence vision, a consistent, generic approachto system integration is needed, that is adapted ...

11 DVI parallel image compression
Michael Tinker
July 1989 **Communications of the ACM**, Volume 32 Issue 7
Full text available: pdf(954.31 KB) Additional Information: full citation, abstract, references, citings, index terms, review

At the heart of DVI is an image compression and expansion technology that uses proprietary chips to expand an image in real time from a bit stream that has been compressed on a large computer at non-real time rates. This article describes how the compression algorithm is used and how it was ported.

12 Optimal latency-throughput tradeoffs for data parallel pipelines
Jaspar Subhlok, Gary Vondran
June 1996 **Proceedings of the eighth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.19 MB) Additional Information: full citation, references, citings, index terms

13 Analysis of replicated data algorithms on processor array architectures
P. J. Narayanan
August 1991 **Proceedings of the 1991 ACM/IEEE conference on Supercomputing**
Full text available: pdf(895.54 KB) Additional Information: full citation, references, citings, index terms

14 Parallel processing image synthesis and anti-aliasing
Richard Weinberg
August 1981 **ACM SIGGRAPH Computer Graphics , Proceedings of the 8th annual conference on Computer graphics and interactive techniques**, Volume 15 Issue 3
Full text available: pdf(834.55 KB) Additional Information: full citation, abstract, references, citings, index terms

The continuing evolution of microelectronics provides the tools for developing new methods of synthesizing digital images by utilizing parallel processing architectures which hold the promise of reliability, flexibility and low cost. Beginning with the earliest real-time flight simulators, parallel processing architectures for image synthesis have been built, but "anti-aliasing" remains a problem. A parallel processing architecture is described and simulated which consists of a serial chain ...

Keywords: Aliasing, Computer graphics, Parallel processing

15 The pixel machine: a parallel image computer
Michael Potmesil, Eric M. Hoffert
July 1989 **ACM SIGGRAPH Computer Graphics , Proceedings of the 16th annual conference on Computer graphics and interactive techniques**, Volume 23 Issue 3

Full text available: pdf(3.12 MB) Additional Information: full citation, abstract, citings, index terms

We describe the system architecture and the programming environment of the Pixel Machine - a parallel image computer with a distributed frame buffer.The architecture of the computer is based on an array of asynchronous MIMD nodes with parallel access to a large frame buffer. The machine consists of a pipeline of *pipe nodes* which execute sequential algorithms and an array of *m* &times; *n* pixel nodes which execute parallel algorithms. A *pixel node* directly accesses e ...

16 Parallel volume ray-casting for unstructured-grid data on distributed-memory architectures
Kwan-Liu Ma
December 1995 **Proceedings of the IEEE symposium on Parallel rendering**
Full text available: pdf(8.60 MB) Additional Information: full citation, citings, index terms

17 PAVLOV: a programmable architecture for volume processing
Kevin Kreeger, Arie Kaufman
August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(1.62 MB) Additional Information: full citation, references, citings, index terms

Keywords: 2D mesh array, SIMD, segmentation, volume processing, volume rendering

18 Optimal mapping of sequences of data parallel tasks
Jaspal Subhlok, Gary Vondran
August 1995 **ACM SIGPLAN Notices , Proceedings of the fifth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 30 Issue 8
Full text available: pdf(1.17 MB) Additional Information: full citation, abstract, references, citings, index terms

Many applications in a variety of domains including digital signal processing, image processing and computer vision are composed of a sequence of tasks that act on a stream of input data sets in a pipelined manner. Recent research has established that these applications are best mapped to a massively parallel machine by dividing the tasks into modules and assigning a subset of the available processors to each module. This paper addresses the problem of optimally mapping such applications on ...

19 A symbolic substitution based parallel architecture and algorithms for high-speed parallel processing
Ahmed Louri
January 1990 **Proceedings of the 1990 ACM annual conference on Cooperation**
Full text available: pdf(754.76 KB) Additional Information: full citation, abstract, references, index terms

A new parallel architecture that is amenable to optical implementation is presented for massively data-parallel computing. The architecture is an SIMD model that exploits spatial parallelism and processes 2-D binary images as fundamental computational entities. Processing is based on a new technique called symbolic substitution logic. A hierarchical mapping technique is presented for designing data-parallel algorithms and mapping them onto the optical architecture. The mapp ...

20 A data distributed, parallel algorithm for ray-traced volume rendering
Kwan Liu Ma, James S. Painter, Charles D. Hansen, Michael F. Krogh
November 1993 **Proceedings of the 1993 symposium on Parallel rendering**
Full text available: pdf(2.85 MB) Additional Information: full citation, references, citings, index terms

Keywords: massively parallel processing, network computing, scientific visualization, volume rendering

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L3	2937350	@ad<"19991101"	USPAT	OR	ON	2005/06/30 17:45
L4	44	2 and 3	USPAT	OR	ON	2005/06/30 17:48
L5	236039	mesh	USPAT	OR	ON	2005/06/30 17:46
L6	2	4 and 5	USPAT	OR	ON	2005/06/30 17:46
L7	15278	operand	USPAT	OR	ON	2005/06/30 17:48
L8	22	4 and 7	USPAT	OR	ON	2005/06/30 17:59
L9	35743	interpolation	USPAT	OR	ON	2005/06/30 17:59
L10	1	8 and 9	USPAT	OR	ON	2005/06/30 18:06
L11	62797	"712"/("20,21,22").ccls.	USPAT	OR	ON	2005/06/30 18:07
L12	1839	first adj operand and second adj operand	USPAT	OR	ON	2005/06/30 18:07
L13	447	11 and 12	USPAT	OR	ON	2005/06/30 18:07
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L15	373	11 and 14	USPAT	OR	ON	2005/06/30 18:08
L16	1364	first adj operand with second adj operand	USPAT	OR	ON	2005/06/30 18:08
L17	303	11 and 16	USPAT	OR	ON	2005/06/30 18:08
L18	668	(first adj operand with second adj operand) same instruction	USPAT	OR	ON	2005/06/30 18:08
L19	198	11 and 18	USPAT	OR	ON	2005/06/30 18:09
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